4E2149

Roll No. _____ [Total No. of Pages : 3

4E2149

B. Tech. IV Semester (Mian/Back) Examination - 2012

Electrical & Electronics Engineering

4EX2 Digital Electronics

BM, EX, EC, EI

Time : 3 Hours

Maximum Marks : 80
Min. Passing Marks : 24

Instructions to Candidates:

*Attempt any **five** questions. Selecting **one** question from **each** unit. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated Clearly).*

Unit - I

1. a) Find the 9's complement of the following decimal numbers 4526.075

   b) Add + 40.75 to - 40.75 using the 12 - bit 2's complement arithmetic

   c) Convert $(378.93)_{10}$ to octal

   d) Convert $(1011011011)_2$ to Hexadecimal

   e) Convert $(756.603)_8$ to Hexadecimal

   f) Add -25 to + 14 using the 8 - bit 1 's complement method

   g) Convert $(2598.675)_{10}$ to Hexadecimal

   h) Subtract the octal number's : 3006.05 - 2657.16 **(2×8=16)**

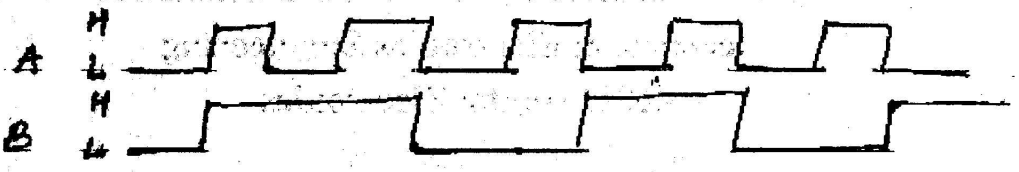
OR

   a) Subtraction in XS - 3 code : 267 - 175 **(2)**

   b) Gray code conversion $(527)_8$ **(2)**

   c) Subtraction in 8421 code using the 10 's complement method 206.40 - 507.60 **(2)**

d) Waveform A and B shown in fig. are applied to a 2 - input NAND, X - NOR, X - OR. Determine the output waveform's (6)



e) Solve this $(a+b+cd)(\bar{a}+b)(\bar{a}+b+c)$ (4)

Unit - II

2. a) Write short notes on interfacing of various logic families.

b) With the help of neat circuit diagram explain the working of two input TTL NAND gate

c) Determine the fan - out the circuit of figure. Also find its noise margine.

(6+4+6)

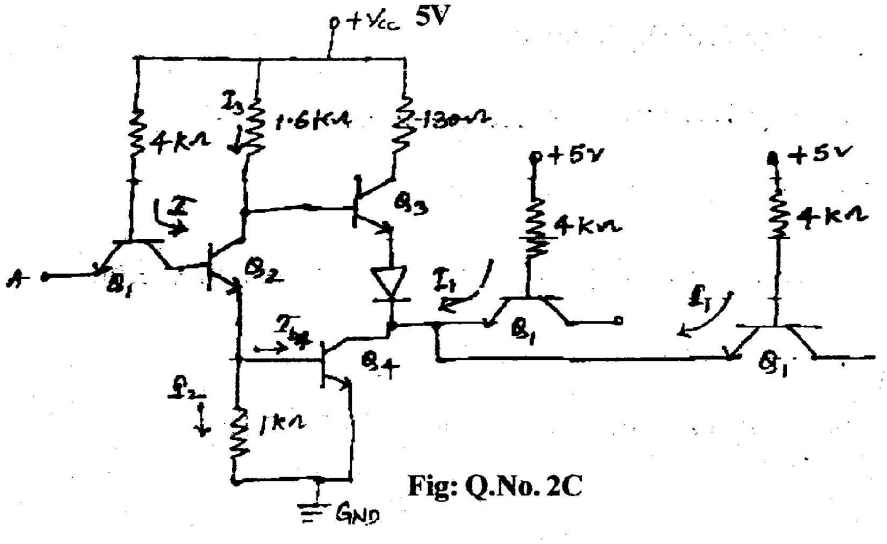


Fig: Q.No. 2C

OR

a) Compare different logic families.

b) Draw in CMOS NAND, NOR, Inverter gate

c) Explain Totem pole arrangement in TTL. What is the advantage and disadvantage of totem pole arrangement. **(6+5+5)**

Unit - III

3. Solve by K - map and Realized by the NAND Gate.

a) $f(A,B,C,D) = AB\bar{C}D + \bar{A}BCD + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} + A\bar{C} + A\bar{B}C + \bar{B}$

b) Solve by K - map and Realized by the NOR Gates.

$f(A,B,C,D) = \pi M(1,2,3,5,6,7,9,10,11,13,14,15)$ **(8+8)**

OR

a) Minimize the following switching function using Quine - Mc Clusky method and realize using NOR/NAND gates. $f(A,B,C,D) = \Sigma(0,2,4,6,9,11,13,14,15)$

b) Minimize the following expression using variable Enter Map $f = \Sigma(\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + ABCD + A\bar{B}CD + A\bar{B}C\bar{D})$. **(8+8)**

Unit - IV

4. a) Design 4 bit carry look ahead adder.

b) Design a binary to gray and gray to binary decoder Circuits. **(8+8)**

OR

a) Implement the following function 16:1 multiplexer $f(A,B,C,D) = \Sigma m(0,1,3,4,6,8,10,11,12,15)$

b) Design a BCD to 7 - Segment code converter circuit. Assume 7 segment display available are of common anode type **(8+8)**

Unit - V

5. a) What do you understand by race around condition? How it's overcome in master slave J - K flip - flop.

b) Explain the operation of various type of shift register. **(8+8)**

OR

a) Draw the 4 - bit a synchronous BCD ripple counter using any suitable flip - flop and Explain the output changes with each clock pulses.

b) Design a type T counter that goes through states 0, 3, 5, 6, 0, ... Is the counter self - starting? **(8+8)**
